Sole Inventor

Docket No. 20059/PIA30957

"EXPRESS MAIL" mailing label No.
EL 995292513 US
Date of Deposit: **November 13, 2003**

I hereby certify that this paper (or fee) is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 CFR §1.10 on the date indicated above and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Magda Greer

Magda Greer

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, In Kyu Chun, a citizen of Korea, residing at 891-10 Daechi-dong, Gangnam-gu, Seoul, Republic of Korea have invented a new and useful **METHOD FOR FORMING A CONTACT USING A DUAL DAMASCENE PROCESS IN SEMICONDUCTOR FABRICATION**, of which the following is a specification.

METHOD FOR FORMING A CONTACT USING A DUAL DAMASCENE PROCESS IN SEMICONDUCTOR FABRICATION

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to a method for fabricating a semiconductor device and, more particularly, to a method for forming a contact of the semiconductor device having a Cu line by using a dual damascene process.

BACKGROUND

[0002] The demand for semiconductor devices having a Cu line has been increasing due to the low resistance of the Cu line. As a result, various types of semiconductor devices having a Cu line have been recently developed. Cu lines are usually deposited on a copper seed layer (e.g., a Ta(Tantalum)/TaN(Tantalum nitride) double layer), which also serves as a Cu diffusion barrier that prevents copper in the Cu line from being diffused, by a dual damascene process.

[0003] However, the contacts of semiconductor devices are usually implemented using a tungsten plug (W-plug) fabricated using a single damascene process instead of a dual damascene process, which is usually used to form the Cu line and a via hole.

[0004] To form the tungsten plug, both a tungsten CMP (chemical mechanical polishing) process and a touch-up process, which is a follow-up process to the tungsten CMP process, are required. However, in the course of the touch-up process, wafer surfaces are often scratched microscopically and macroscopically and insulating layers are often ripped out by oxide particles.

[0005] Moreover, the Ta/TaN double layer, which serves as the Cu diffusion barrier at an interface between the tungsten plug and the Cu line, may collapse in the

course of a Cu CMP process due to a void (i.e., a vacant region in the tungsten plug) generated during a tungsten CVD (chemical vapor deposition) process.

[0006] Figs. 1A to 1F show a conventional method for forming a contact using the tungsten plug and the single damascene process, sequentially. As shown in Fig. 1A, a PMD (pre-metal dielectric) layer 102 is photo-lithographically etched to form a contact hole 104. Thereafter, as shown in Fig. 1B, a tungsten diffusion barrier 106 (e.g., a Ti(Titanium)/TiN(Titanium nitride) double layer) is deposited on the PMD layer 102 and sidewalls and an undersurface of the contact hole 104, and then a tungsten layer 108 is deposited on the tungsten diffusion barrier 106 by the tungsten CVD process.

[0007] In the course of the CVD process, the tungsten layer 108 begins to grow from the sidewalls of the contact hole 104 so that the void can be produced at the center of the contact hole 104.

[0008] Then, as shown in Fig. 1C, the tungsten layer 108 and the tungsten diffusion barrier 106 above the PMD layer 102 are removed by the tungsten CMP process and the touch-up process to form a tungsten plug 109, which has substantially the same height as that of the PMD layer 102. The tungsten layer 108 is polished by the tungsten CMP process and, tungsten residue, which was not completely removed during the tungsten CMP process, is removed by the touch-up process (e.g., an oxide CMP process). Thereafter, as shown in Fig. 1D, an additional PMD layer 103 is deposited on both sides of the PMD layer 102 to form a trench 110 having a width greater than that of the tungsten plug 109.

[0009] Then, as shown in Fig. 1E, a Cu diffusion barrier 111 (e.g., a Ta/TaN double layer) is deposited on the additional PMD layer 103 and sidewalls and an undersurface of the trench 110, and then copper 112 is deposited on the Cu diffusion

barrier 111. Then, as shown in Fig. 1F, the copper 112 over the trench 110 is removed by a Cu CMP process to form a Cu line 113.

[0010] The above-described conventional method must utilize the touch-up process because the additional PMD layer 103 should be deposited on a clean surface of the PMD layer 102 to reduce a leakage current that may be caused by tungsten residue remaining at an interface of the PMD layers 102 and 103. However, as noted above, the wafer surfaces may be scratched microscopically and macroscopically and the insulating layers may be ripped out during the touch-up process.

[0011] Further, with the above-described conventional method, the void can be exposed after the tungsten CMP process or the touch-up process so that the Cu diffusion barrier 111 cannot be deposited over the void. Thus, in the course of the Cu CMP process, the copper in the Cu line 113 can be diffused to the silicon substrate 100 via the tungsten diffusion barrier 106 which cannot serve as the Cu diffusion barrier. Even if the void is not exposed after the tungsten CMP process or the touch-up process, the Cu diffusion barrier 111 may collapse to thereby expose the void by a pressure exerted during the Cu CMP process, so that the copper in the Cu line 113 can be diffused to the silicon substrate 100 via the tungsten diffusion barrier 106 in the same way.

[0012] Still further, with the above-described conventional method, the contact resistance between the tungsten plug 109 and the Cu line 113 is high because the width of the contact region therebetween is narrow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figs. 1A to 1F show a conventional method for forming a contact during a semiconductor fabrication process.

[0014] Figs. 2A to 2G depict an example method for forming a contact using dual damascene process during fabrication of a semiconductor.

DETAILED DESCRIPTION

[0015] As described in greater detail below, an example method for forming a contact of a semiconductor device having a Cu line uses a dual damascene process to reduce scratches on wafer surfaces, reduce a rip-out defect at an insulating layer, release a diffusion phenomenon of a copper due to collapse of a Cu diffusion barrier, and to reduce a contact resistance between a tungsten plug and the Cu line.

[0016] Figs. 2A to 2G depict an example method for forming a contact by using a dual damascene process during fabrication of a semiconductor. As shown in Fig. 2A, a PMD layer 202 is photo-lithographically etched to form a dual damascene pattern 201. The dual damascene pattern 201 includes a contact hole portion located at a lower part thereof and a trench portion located at a upper part thereof. The underside of the contact hole portion is in contact with a silicon substrate 200. Because the width of the trench portion is wider than that of the contact hole portion, the underside of the trench portion is in contact with the contact hole portion and the PMD layer 202. Then, as shown in Fig. 2B, a tungsten diffusion barrier 204 (e.g., a Ti/TiN double layer) is deposited on the dual damascene pattern 201 (i.e., on the PMD layer 202) on sidewalls of the contact hole portion and the trench portion and on the underside of the contact hole portion and the trench portion. It is preferable that the thickness of Ti/TiN is 30/5 nm.

[0017] Thereafter, as shown in Fig. 2C, a tungsten layer 206 is deposited on the tungsten diffusion barrier 204 by a tungsten CVD (chemical vapor deposition) process to fill the contact hole portion and the trench portion.

[0018] Then, the tungsten layer 206 outside of the trench portion is removed as shown in Fig. 2D and an upper part of the tungsten layer 206 in the trench portion is removed as shown in Fig. 2E, by a dry etching process, to form a tungsten plug 207. Thus, the tungsten plug 207 occupies the contact hole portion and the lower part of the trench portion so that a void, i.e., a vacant region in the contact hole portion, generated during the tungsten CVD process, cannot be exposed. It is preferable that the height of the tungsten plug 207 is 300nm and the diameters of tungsten plug 207 in the contact hole portion and in the lower part of the trench portion are 185nm and 500nm, respectively. Furthermore, because there is no need to deposit an additive layer, such as an additive PMD layer 103 of Fig. 1D, on the PMD layer 202, a touch-up process is not required at the time the tungsten layer 206 is removed. Because there is no touch-up process, the wafer surfaces cannot be scratched thereby.

[0019] Thereafter, as shown in Fig. 2F, a Cu diffusion barrier 205, e.g., a Ta/TaN double layer, is deposited on the PMD layer 202 and on the tungsten plug 207. It is preferable that the thickness of Ta/TaN is 7.7/7.5 nm. Beacuse the void in the contact hole portion is not exposed, the Cu diffusion barrier 205 can be deposited on the whole surface of the tungsten plug 207. Then a copper layer 208 is deposited on the Cu diffusion barrier 205 and, as shown in Fig. 2G, the copper layer 208 outside of the trench portion is then removed by a Cu CMP process to form a Cu line 209. It is preferable that the height of the Cu line 209 is 250nm.

[0020] In spite of a pressure exerted by the Cu CMP process, the Cu diffusion barrier 205 does not collapse easily because the void in the contact hole portion is not exposed by the tungsten plug 207 and the Cu diffusion barrier 205 can be deposited on the whole surface of the tungsten plug 207.

[0021] Additionally, a contact resistance between the tungsten plug 207 and the Cu line 209 is lower than that of the conventional method described in connection with Fig. 1 because the width of an interface between the tungsten plug 207 and the Cu line 209 is wide.

[0022] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.